Demonstration of Improved Heteroepitaxy, Scaled Gate Stack and Reduced Interface States Enabling Heterojunction Tunnel FETs with High Drive Current and High On-Off Ratio

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Abstract: Staggered tunnel junction ($GaAs_{0.35}Sb_{0.65}$ /$In_{0.7}Ga_{0.3}As$) is used to demonstrate heterojunction tunnel FET (TFET) with the highest drive current, I_{on}, of 135μA/μm and highest I_{on}/I_{off} ratio of 2.7×10^4 (V_{ds}=0.5V, V_{on}-V_{off}=1.5V). Effective oxide thickness (EOT) scaling (using Al_2O_3/HfO_2 bilayer gate stack) coupled with pulsed I-V measurements (suppressing D_{it} response) enable demonstration of steeper switching TFET.

Introduction: Mixed arsenide-antimonide based lattice-matched heterojunction provides a wide range of compositionally tunable effective tunneling barrier height (Eb_{eff}), from 0.5eV to 0eV [4,7]. With increasing Sb and As composition, Eb_{eff} reduces and TFET I_{on} can approach MOSFET level without compromising the high I_{on}/I_{off} ratio [3-5]. However, engineering an abrupt change from Sb rich to As rich interface is a significant growth challenge [3]. The objectives of this work are three fold: 1) we explore proper growth switching conditions to control the atomic termination at the $GaAs_{0.35}Sb_{0.65}/In_{0.7}Ga_{0.3}As$ interface to reduce defects and demonstrate TFET with higher I_{on}/I_{off} ratio than reported before [3]; 2) we demonstrate the effect of EOT scaling on TFET switching slope (SS) enhancement; 3) finally, we employ ultra-fast pulsed I-V measurement to mitigate the interface state (D_{it}) response in order to improve the TFET SS and I_{on}/I_{off} ratio over a specified gate voltage (V_{gs}) swing.

Materials Characterization: Figs. 1(a-c) show the schematic layer structures for $In_{0.7}Ga_{0.3}As$ HomJ, as well as $GaAs_{1-x}Sb_x$/ $In_yGa_{1-y}As$ Moderate and High HetJ TFETs for x=0.6,0.65 and y=0.65,0.7 respectively, grown on semi-insulating InP substrate using solid-source molecular beam epitaxy. For the High HetJ TFET structure, two wafers were grown to study the impact of (a) GaAs-like and (b) InAs-like surface termination while switching from Sb-rich $GaAs_{0.35}Sb_{0.65}$ to As-rich $In_{0.7}Ga_{0.3}As$ layer. For the latter case, while ramping up the As flux from 35% to 100%, 1-2 ML of Indium (In) was added prior to $In_{0.7}Ga_{0.3}As$ layer. Figs. 2 (a,b) show asymmetric (115) reciprocal space maps of the High HetJ TFET structures. In both cases, the growth of the metamorphic buffer results in an $In_{0.65}Al_{0.35}As$ "virtual" substrate with ≥90% strain relaxation. However, the subsequent $GaAs_{0.35}Sb_{0.65}$ and $In_{0.7}Ga_{0.3}As$ active device layers differ in their strain with respect to the "virtual" substrate. With the GaAs terminated heterointerface, the active layers are strain relaxed and susceptible to defect formation, whereas the device layers on the InAs terminated interface are pseudomorphic to the $In_{0.65}Al_{0.35}As$ "virtual substrate" and likely "defect-free". This is evident in Fig. 2 (c,d) where atomic force microscopy (AFM) images reveal lower surface roughness (4.5nm) and 2D cross-hatch pattern for InAs terminated wafer compared to the GaAs terminated one (with roughness of 5.6nm and no cross-hatch pattern).

Device Characterization: The vertical TFET fabrication process is described in [4]. Fig. 1(d) shows the cross-sectional TEM micrograph of the fabricated High Hetj TFET. Figs. 2 (e,f) compare the I_{ds}-V_{gs} and I_{ds}-V_{ds} characteristics for the high HetJ TFET with GaAs and InAs surface termination. More than 3 orders in magnitude improvement in I_{on}/I_{off} ratio is achieved with the latter due to the reduction in defect assisted conduction. The improvement in heteroepitaxy with InAs termination is reflected in the improved electrostatics (smaller SS and DIBT) for the same device geometry. Figs. 1(e-i) compare the performance of the High HetJ TFET with Mod. HetJ and HomJ TFETs. First, I_{on} progressively increases by 325% with decreasing Eb_{eff} (from 0.58eV to 0.25eV) due to the increase in tunneling transmission coefficient. Second, the drain induced barrier thinning (DIBT) improves with reducing Eb_{eff} due to inter-band generation occurring closer to the source/channel junction, thus improving device electrostatics [5]. The SS vs I_{ds} curve also shifts with reducing Eb_{eff}, with the minimum SS occurring at higher I_{ds} which is essential for TFET operation with MOSFET like performance. To further enhance performance, we scaled the EOT for the High HetJ TFET, from 2nm to 1.75nm, and reduced the V_{gs} window by 0.5V for the same I_{on}-I_{off} (Fig. 3a). Figs. 3(b,c) summarize the improvement in both I_{on} (tunneling transmission) and DIBT (electrostatics) as a function of Eb_{eff} and EOT. The switching slope, SS, in all fabricated devices is greater than 60mV/dec at room temperature and is caused by the presence of interface states (D_{it}) at the high-κ/channel interface [1,3-5]. We perform ultra-fast pulsed I_{ds}-V_{gs} measurements on the HomJ TFET with input gate voltage pulses having rise time (t_r) of 10ns, to suppress D_{it} response. The TFET I_{ds} response was then reliably sampled after 150ns (t_{meas}). The pulsed I_{ds}-V_{gs} measurement (Figs. 4(a,b)) show marked steepening of the switching slope (SS) with minimum SS of 100mV/decade and matches the theoretical I_{ds}-V_{gs} for $D_{it}\sim 8\times10^{11}/cm^2$ [7]. The pulsed I_{ds}-V_{gs} study allows us to accurately predict the performance realizable in High HetJ TFET with similar D_{it} $\sim8\times10^{11}/cm^2$ and EOT of 1nm (Figs. 5(a,b)). Two dimensional device simulations show that high Hetj TFET can maintain sub kT/q SS over two orders of magnitude of drain current (10^{-9} to 10^{-7} A/μm). Heterojunction Tunnel FET can deliver MOSFET-like performance with better I_{on}/I_{off}, making them a promising post CMOS candidate for low power, high performance applications.

Summary: Table 1 benchmarks the on current (I_{on}), on-off ratio (I_{on}/I_{off}) and effective switching slope (SS_{eff}) of TFETs, demonstrated till date. The High HetJ TFET in this work shows I_{on} of 135μA/μm and I_{on}/I_{off} $>10^4$ at V_{ds}=0.5V and V_{on}-V_{off}=1.5V. This is the highest ever reported I_{on}/I_{off} ratio for I_{on}> 100μA/μm in the category of TFETs.

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References

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[4]Mohata et. al, DRC, 2011
[5] Mohata et. al, APEX, 2011
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Fabrication and Electrical Characterization

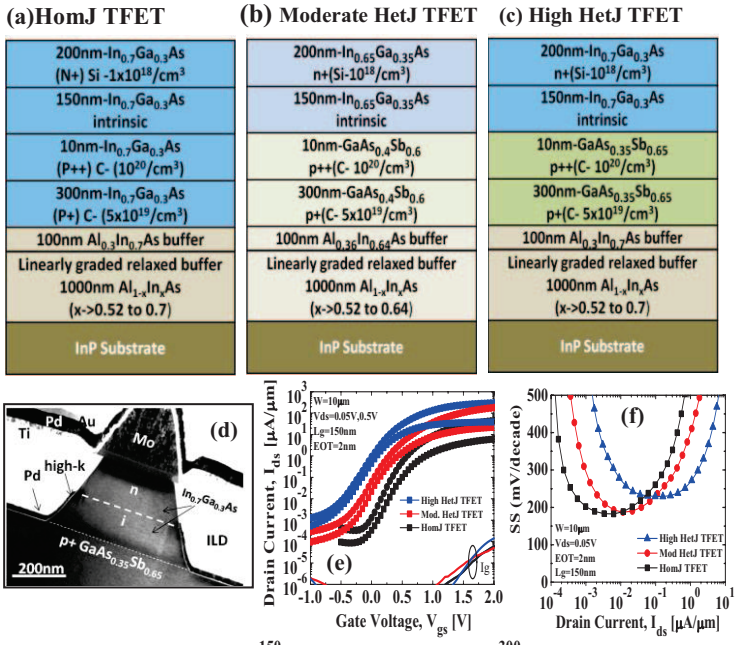

Figure 1-(a-c) TFET layer structures. **(d)** High HetJ TFET cross-section TEM micrograph. **(e-i)** Measured I_{ds}-V_{gs}, I_{ds}-V_{ds} and extracted switching slope (SS) vs I_{ds} characteristics for the three fabricated devices.

EOT scaling (Experimental)

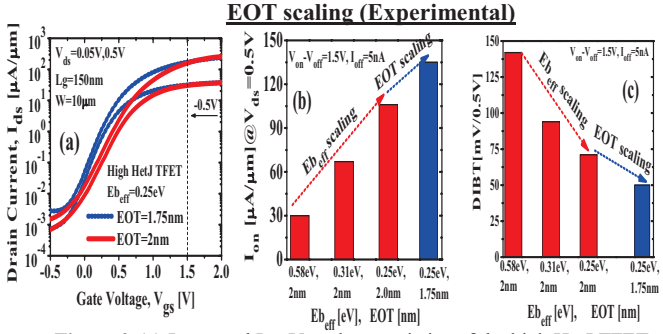

Figure 3-(a) Improved I_{ds}-V_{gs} characteristics of the high HetJ TFET with EOT scaling. **(b,c)** Summary of improvement in measured I_{on} and Drain Induced Barrier Thinning (DIBT) with Eb_{eff} and EOT scaling. DIBT improves with increasing stagger due to interband generation occurring closer to the source-channel interface [5].

Further EOT scaling in high HetJ TFET (Exp., Model & Projection)

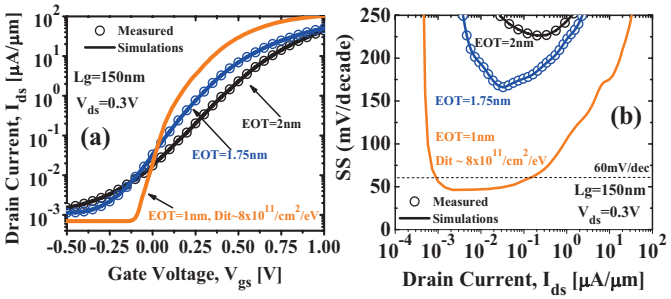

Figure 5-(a,b) An improvement in high-k/channel interface (D_{it} ~$8x10^{11}$/cm^2/eV) combined with further EOT scaling would enable MOSFET-like TFET operation at low V_{cc} with higher I_{on}/I_{off} ratio.

Materials Growth Improvement

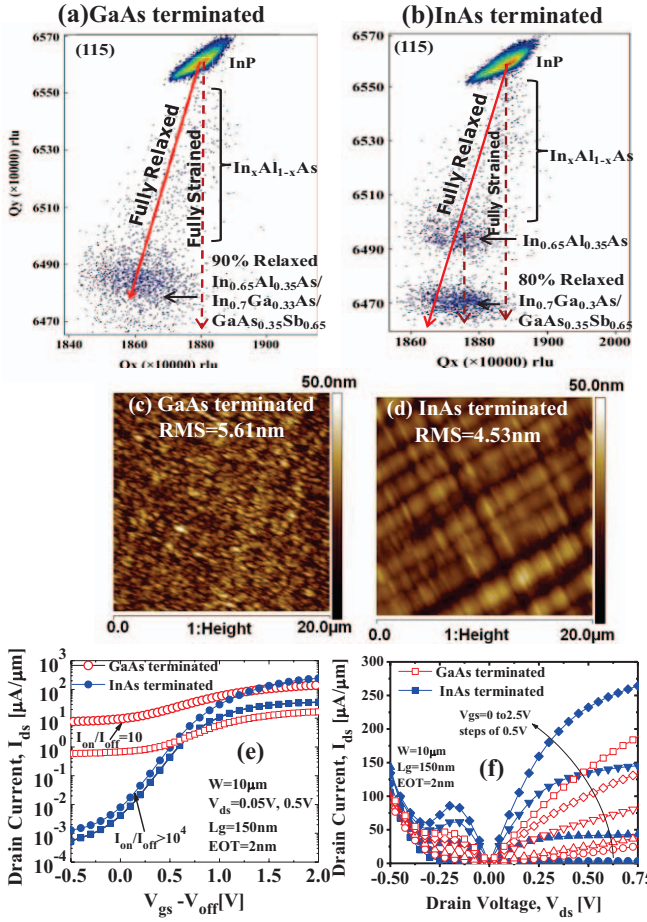

Figure 2- **(a,b)** Asymmetric (115) reciprocal space map and **(c,d)** 20x20 μm^2 atomic force microscopy image of High HetJ TFET layers for the cases with GaAs and InAs terminated hetero-interfaces; **(e,f)** Improvement in I_{ds}-V_{gs} and I_{ds}-V_{ds} characteristics with InAs terminated hetero-interface.

Minimizing Dit response using Fast I-V (HomJ TFET)

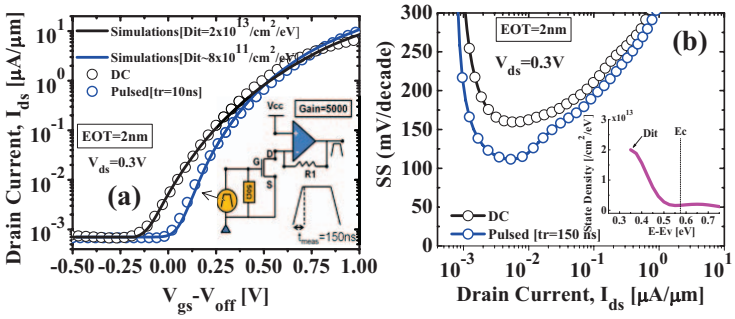

Figure 4-(a) Pulsed I_{ds}-V_{gs} measured on HomJ TFET showing steeper switching by avoiding slow D_{it} response. Inset shows simplified pulsed I-V set-up. **(b)** SS vs I_{ds} showing improved SS minimum with pulsing. Inset shows D_{it} profile used to model DC and pulsed I_{ds}-V_{gs} measurements.

Reference	Eb_{eff} (eV)	Lg (nm)	EOT (nm)	V_{on}-V_{off} (V)	Vds (V)	Ion (μA/μm)	Ion/Ioff	SS_{eff} (mV/dec)
Zhao et. al, EDL,2011 [1]	0.58	100	1.2	1.5	0.5	30	$6x10^3$	200
Dewey et. al IEDM, 2011 [2]	0.74	100	1.1	0.9	0.3	8	$1.6x10^3$	140
Dewey et. al IEDM,2011 [2]	0.58	100	1.1	0.9	0.3	17	$3.4x10^3$	106
Mohata et. al IEDM, 2011 [3]	0.25	150	2	1.5	0.5	135	10	750
HomJ (This work)	0.58	150	2	1.5	0.5	30	$6x10^3$	200
Mod. HetJ (This work)	0.31	150	1.75	1.5	0.5	78	$1.5x10^4$	179
High HetJ (This work)	0.25	150	1.75	1.5	0.5	135	$2.7x10^4$	169

Table 1- Benchmarking I_{on} and I_{on}/I_{off} at V_{ds}=0.5V, I_{off}=5nA/μm [ITRS-2010], where SS_{eff}=(V_{on}-V_{off})/[2log(I_{on}/I_{off})][6]